

# An automated model based design flow for the design of robust CAN FD networks

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**CAN FD addresses the increasing demands on automotive system bandwidth offering an easier adaptability and high re-use factor of existing CAN, the most disseminated in-vehicle network protocol. However, it brings new challenges to the designers. Since the dynamic behavior of the system cannot be predicted by manual calculations, the developers are required to use the simulation to analyze the network design for a robust layout and to investigate the influences of new components with two main goals: improving the signal quality and ensuring a correct communication with precise results even under worst case environmental conditions. Simulation is the only choice to determine the asymmetry of the bits caused by physical layer effects. In order to obtain a design of robust CAN-FD networks, developers are faced with a lot of variations causing a significant amount of data to be analyzed and therefore automatization is a decisive factor to address it properly.**

This paper shows how to define and develop a robust design methodology based on a virtual prototype implementation of the CAN FD networks, which criteria shall be considered and how the entire design flow can be automated to get the most out of the simulation, while decreasing the analysis periods and costs.

CAN FD is a further building block, helping to close the gap between the growing needs regarding the exchange of information from electronic units and the currently available technologies. CAN FD is indeed based on the well-known CAN 2.0b technology but additional criteria need to be considered for the topology validation.

This paper also depicts an automated design flow which is based on simulation, measurements and verification of topologies design. Its main focus is the CAN FD protocol which is a new version of the classical CAN protocol and allows transmitting larger payloads even at higher frequency.

The design flow consists of 3 main steps, whose may be classified in topology simulation, laboratory measurements and verification.

The main objective of this paper is to describe the importance that simulation is acquiring nowadays due to a constant increase of

quality and performance requirements within in-vehicle networks (IVN). Physical layer analysis is the key to obtain a robust design.

One question coming from a designer may be: "Why should I simulate?", which results in the following simulation advantages:

- Quality assurance
- Broader analysis compared to laboratory test(s)
- Total cost reduction

## Topology validation through simulation

The first and most important phase in validating a modern topology design is the simulation phase. The trend shows an ever increasing evaluation of vehicle networks using simulation.

With the need of simulations of CAN FD networks, this trend will be further intensified. The main goal of the simulation is to achieve a confidence level on the designed topology. Once the design is approved, the design can be implemented in either a laboratory or in a vehicle.

Simulation involves accurate models [1] for transceivers and cables as well as a simulation environment, controllable by means of scripting, thus automatization.

A previous requirement to the topology simulation is the model development. After having a plausible model, the topology design verification can be executed.

**Model development**

The development of a model is an important step in the design verification flow. Both Figure 1 and Figure 2 show a specific test where the recessive to dominant edge of the model is evaluated for high and low temperatures respectively. The simulation is compared with laboratory measurements and it must reflect the curve shaping of the real device. This test is executed for a device with its typical load conditions.

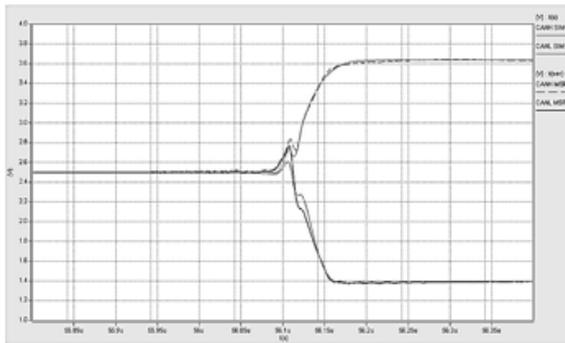


Figure 1: Model verification (high temp.)

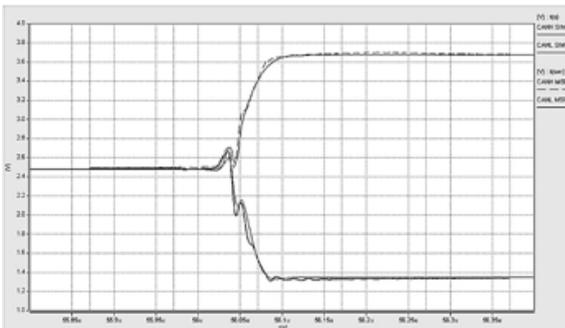


Figure 2: Model verification (low temp.)

On the other side, when the model shows the same behavior as the real device, a test within a network must be executed, consisting once more in the comparison between the simulation and the real measurements. Figure 3 shows an example of a model verification where 8 nodes are connected in a star topology and each stub length is defined as described in [2]. Then the results are compared to laboratory measurements as verification of the behavior within a network. Figure 4 shows a

comparison for common mode signal (CM), differential signal (CAND) and both high and low channels of CAN (CANH and CANL) at the 8th node, observing the settle time in dominant to recessive edge.

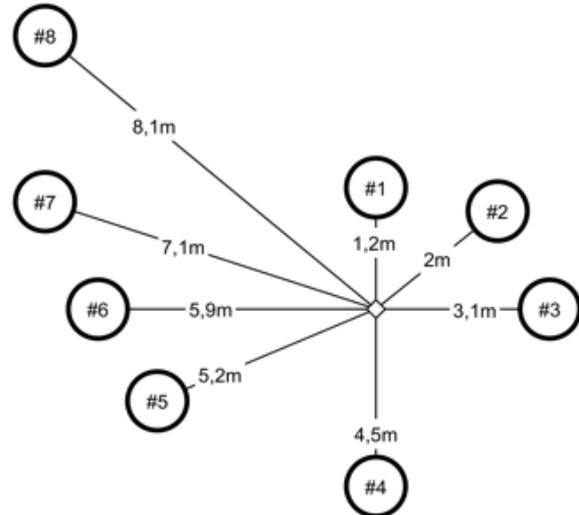


Figure 3: Model verification test network

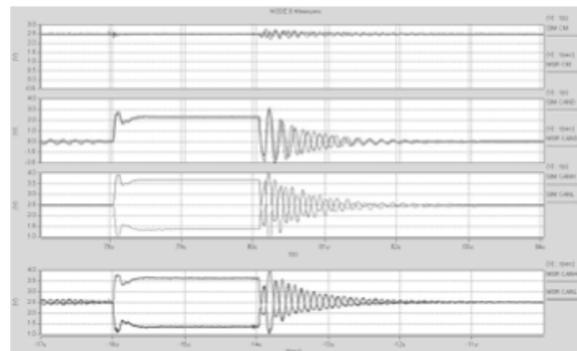


Figure 4: Settle time in dominant to recessive edge at the 8th node

**Topology design verification**

The main goal from the designer’s point of view is to achieve a quality assurance of its own design. Within our typical design flow this is not only feasible but quantifiable. The robustness of the system is evaluated here. The final results should be compared with some specific laboratory measurements.

Particularly in CAN FD networks, the use of simulation is mandatory since the asymmetry of the signal edges plays a very important role due to the possible higher transmission rates during the data phase in relation to the arbitration phase, in comparison to the conventional, classic CAN.

Marginal environmental conditions, such as high or low temperatures, can additionally intensify negative effects on the asymmetry of the signal edges, which can be analyzed easily by simulation.

Since CAN FD is based on the classic CAN, the arbitration is to be considered equal. The same rules and limits for the arbitration phase, as in the classic CAN, are still valid. In this document such rules are not contemplated. However, new additional rules shall be considered for the data phase of the CAN FD in order to judge the above-mentioned asymmetry of the signal edges. The asymmetries of the measured edges within a CAN FD network essentially determine the choice of the sampling point during the data phase.

A round robin communication will be initiated at the simulation of the topology. Each node acts once as a transmitter one after the other and sends a simple pattern to the CAN bus (Figure 5). The pattern generator creates a digital input signal to the TXD pin of the transceiver with the required data rate, over the entire system.

The resulting signals at the digital and analogous side were logged for a subsequent signal processing. With all of the collected signals, it is possible to calculate the propagation delay as well as the differential CAN bus signal level. The quality of the CAN bus signal is analyzed at each node within the topology.

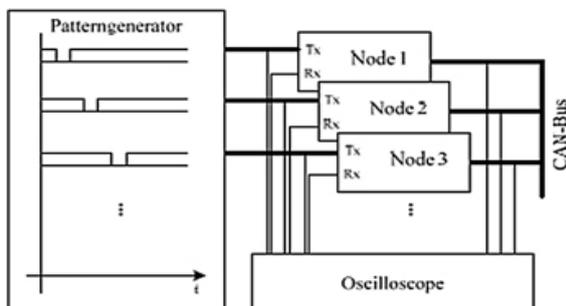


Figure 5: Test pattern generation

### Stimulus signals

The stimulus pattern for each active transmitting ECU is a simple combination of consecutive bits. Depending on the test

case, the bit stream contains one or several logical high bit (1'), followed by one or several logical low (0') bit. A typical scenario is used when 5 dominant bits are followed by a unique recessive bit, then again a few more bits with dominant state.

The combination of five consecutive dominant bits and a recessive bit assures the worst condition after charging the capacitances in the network for a total time equivalent to the five consecutive dominant bits and then discharge the capacitances only during one bit wide. If there is ringing in the network, this condition should expose it at its worst condition. In this way, the recessive bit ( $t_{REC}$ ) is in between two dominant bits and the receiver must be able to detect this recessive bit.

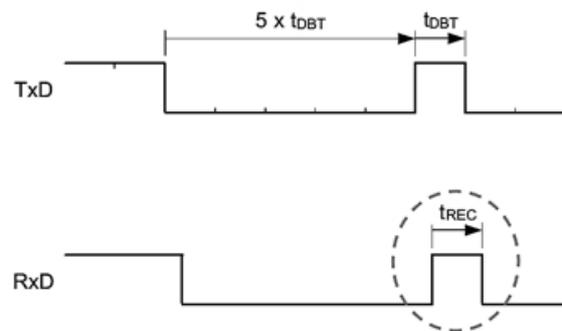


Figure 6: Stimulus at TxD and measurement at RxD

### Validation criteria

The most important criteria for a correct communication are:

- clock tolerance, which depends on the bit timing [3]
- Safe sampling of each bit.

While the requirements for clock tolerance concentrate on the bit timing only and do not involve topology effects, the safe sampling of each bit is focused on the different propagation delays for a dominant to recessive edge and vice versa. The higher the baud rate is the more important the symmetry between the propagation delays of both edges becomes. This leads to an especial analysis regarding the timing components a transmission from one node to another requires.

**Clock tolerance**

In today’s applications there is no separate clock for the CAN controller. The clock is derived from the CPU clock. This clock is generated by a crystal or ceramic resonator with a frequency  $f_{CPU}$  and has its typical clock tolerance. Sometimes it is needful to use a PLL to adapt the clock to the CAN controller’s requirements, but dividing or multiplying the clock affects the clock tolerance too. Knowing the clock tolerance for each node is a starting point and it is recommended to check the inequalities described in [3]. Depending on the tolerance range for a CAN controller’s clock frequency  $f_{CAN}$  around the nominal frequency  $f_{nom}$  with:

$$(1 - df) < \frac{f_{CAN}}{f_{nom}} < (1 + df)$$

and on the bit time settings of each node, the maximal allowed time for signal propagation is fixed.

**Safe sampling**

The following delays are represented by the  $t_{SLOPE}$  slope delay shown in Figure 7:

- $t_{CC,T}$  Delay of the CAN communication controller for internally activating the transmitted bit until available on the output pin,
- $t_{TRX,T}$  Transmitter delay of the transceiver from changing the input signal until first recognizing on the output pin,
- $t_{WIRE}$  Wiring propagation delay,
- $t_{TRX,R}$  Receiver delay of the transceiver from crossing the threshold voltage until changing the output pin,
- $t_{CC,R}$  Delay of the CAN communication controller from changing the input signal until internally recognizing.

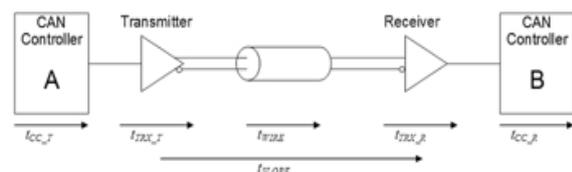


Figure 7: Node to node components

A failure-free operation of a CAN FD network depends on the one hand on a correct

re-synchronization and on the other hand on a correct sampling of each bit of a CAN FD frame. Both shall be ensured for the differed fields of a CAN frame. Under the condition of a regular network communication, a couple of different scenarios shall be taken into consideration.

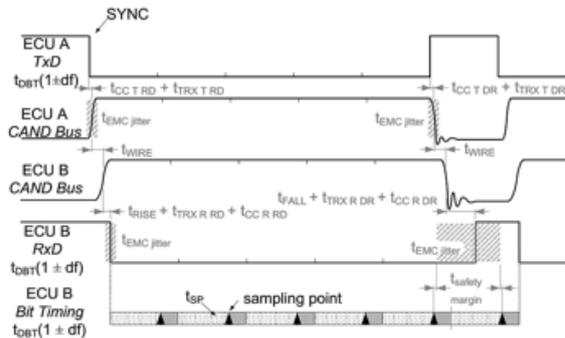


Figure 8: Node to node timing

To ensure the robustness of CAN FD, a safety margin before and after the sampling point shall be considered.

The safety margin in front of the sampling point can be considered as the minimal distance between the received edge at the beginning of the ideal bit and the sample point. In the same way, the safety margin after the sampling point is considered as the minimal distance between the sample point and the received edge at the end of the ideal bit.

The measured recessive bit time  $t_{REC}$  is taken as the nominal bit time minus all the following parameters in the signal:

$$t_{REC} = t_{BIT_D} - (t_{TX-T_{d2r}} - t_{TX-T_{r2d}}) - (t_{TX-R_{d2r}} - t_{TX-R_{r2d}}) - (t_{d2r} - t_{r2d})$$

- $t_{REC}$ : Measured recessive time
- $t_{BIT_D}$ : The time of a bit in data phase
- $TX$ : Transceiver delay
- $T$ : Transmitting
- $R$ : Receiving
- $d2r$ : Dominant to recessive edge
- $r2d$ : Recessive to dominant edge

With that said, taking Figure 6 as reference and by observing  $t_{REC}$ , following inequalities are to be contemplated:

- Supposing that node A is faster than node B, at the 5th bit of the observed RxD signal at node B should be

$$t_{REC} < t_{BIT_D} + t_{SP(df_{B+})} + t_{CC} - t_{CLK} - t_{SM}$$

- Supposing that node A is slower than node B, at the 6th bit of the observed RxD signal at node B should be

$$t_{REC} > t_{SP(df_{B-})} + t_{CC} + t_{CLK} + t_{SM}$$

$t_{SM}$ : Safetymargin including factors as clock jitter, CAN controller execution time and EMC jitter

$t_{SP}$ : Sample point time within a bit

$df_{B+/-}$ : Index to indicate that the frequency is deviated due to clock deviation

$t_{CC}$ : Controller processing time

$t_{CLK}$ : Clock tolerance influence

With both inequalities,  $t_{REC}$  is bounded between a minimum and a maximum possible value. A safe sampling test evaluation should be able to detect if  $t_{REC}$  is out of boundaries and report this in the verdict.

Figure 9 shows an example where  $t_{REC}$  is too small following the exposed rules. For this particular case, the bit time is 500 ns and  $t_{REC}$  should be more than 331 ns. The measurement shows a value of 318 ns thus the minimum is not satisfied. This will be reported as a FAIL condition for this topology. The same is applied if the recessive time results are too large.

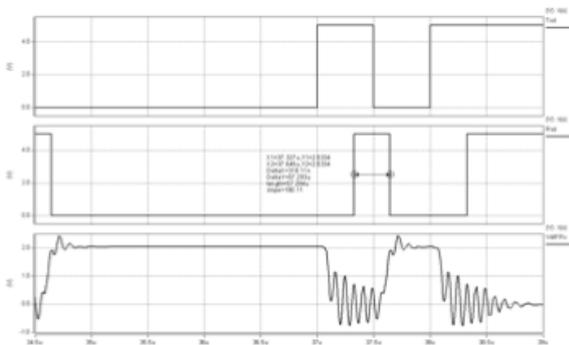


Figure 9: example with  $t_{REC}$  too small

### Settle time

Settle time is an important measurement to be taken. The important edge here is the edge from dominant state to recessive state in the bus. You can either measure

the falling time of the signal from the higher threshold to the lower threshold or to make the same measurement but including the 5 dominant bits before changing to recessive state as shown in Figure 10.

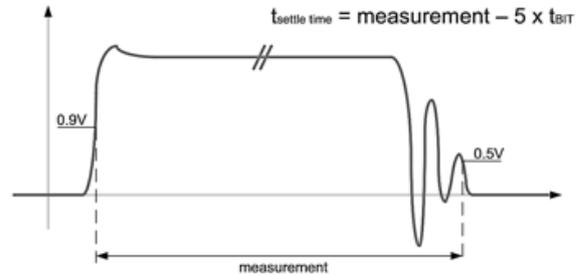


Figure 10: Settle time evaluation

The criterion here is to observe if the settle time occurs before a sample point and even before of a half bit. The percent values with respect to a bit time used for this evaluation are  $SP_{\%}$  and 50% respectively.

$$\frac{(t_{settle} - 5 * t_{BIT})}{t_{BIT}} \left\{ \begin{array}{l} > SP_{\%} \rightarrow \text{not ok} \\ > 50\% \text{ and } < SP_{\%} \rightarrow \text{warning} \\ < 50\% \rightarrow \text{ok} \end{array} \right.$$

Table 1 as well as Figure 11 show an example on how an output of the simulation may be. In this case we observe 3 settle time measurements between 3 nodes where ECU1 is the transmitter. The loop behavior for ECU1 is not passing the test due to ringing while the connection between ECU1 and ECU4 is on the warning area and at the same time the connection between ECU1 and ECU19 is successful.

Table 1: Example of simulation outputs

TX node	RX node	Measure	Limit	Verdict
ECU <sub>1</sub>	ECU <sub>1</sub>	421 [ns]	400 [ns]	FAIL
ECU <sub>1</sub>	ECU <sub>4</sub>	345 [ns]		WARN.
ECU <sub>1</sub>	ECU <sub>19</sub>	32 [ns]		PASS

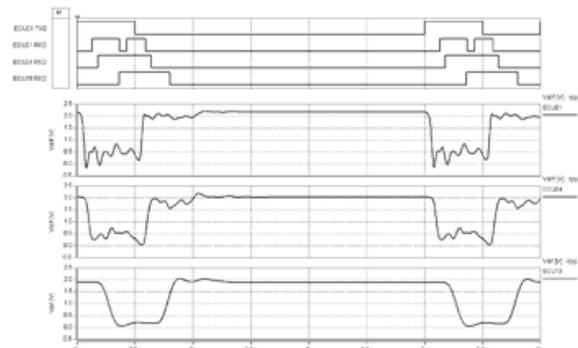


Figure 11: Signals related to Table 1

**Confidence level achievement**

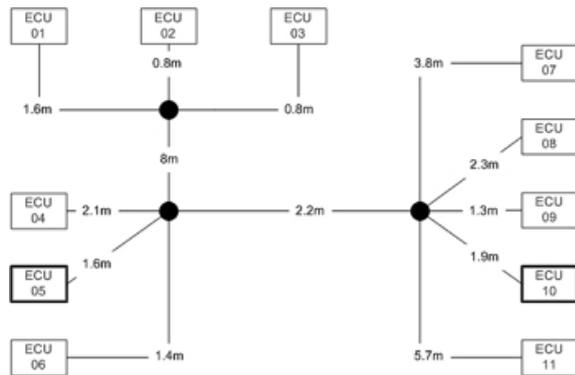


Figure 12: Topology with 11 nodes

The designer may be interested in achieving a certain degree of confidence after simulation results thus the next step in this direction is to execute some laboratory measurements. Figure 13 shows a comparison between simulation and measurement of the settle time at the 7th node in the topology shown in Figure 12.

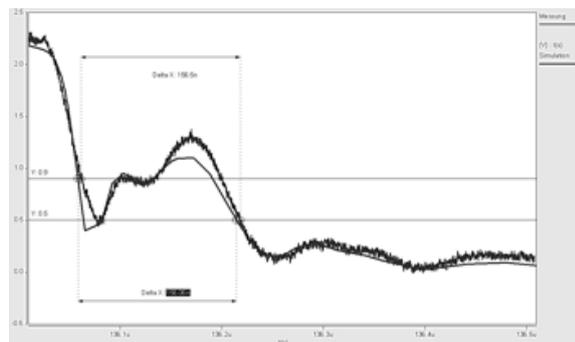


Figure 13: Measurement vs. simulation

Some communication simulation as well as measurements may be tested, thus creating a table similar to Table 2.

Table 2: Simulation and measurements baud

Baude rate [Mb/s]	Simulation	Measurement
0.5	PASS	PASS
1	PASS	PASS
2	PASS <sup>1</sup>	PASS <sup>1</sup>
3	FAIL	FAIL
4	FAIL	FAIL
5	FAIL	FAIL

In the following sections a special overview regarding automatization in simulation is contemplated.

**Need for automatization**

Up to this point of the paper, we have covered the simulation validation for topology designs which shows a highly recommendable practice to verify designs. Now we are able to discuss the applications that the industry demands nowadays and to justify why a simulation environment should be automatized.

It is worth to mention that the maximum baud rate depends on the target topology, i.e. each topology needs to be validated at a certain baud rate. Suppose that we consider evaluating a topology with 12 electronic control units (ECU), that is  $n=12$ . At the same time we usefully consider to evaluate this topology in 2Mbit/s and 5Mbit/s. A manufacturer aims to distribute this product in different applications and even different parts of the world, thus demanding different temperature scenarios. Here we can consider the temperature limits of an automotive application as minimal temperature (MIN), room temperature (TYP) and high temperature (MAX). With a kind of test as described in section I.b, we generate  $n^2$  signals to be evaluated and this for 3 different temperature scenarios. For each signal, 4 measurements should be taken for each combination of rising/falling edges, i.e. one measurement will be from recessive to dominant edge (R2D) at the transmitter (TX) side to the R2D at the receiver side (RX), the other measurement will be from R2D at the TX side to the dominant to recessive edge (D2R) at the RX side. The other two measurements are the D2R at the TX side to both D2R and R2D at the RX side. The total required process gives a total of  $2(freq.) * 4(meas.) * 3(temp.) * n^2 = 3456$  measurements!

Maybe a person can do this process alone or working in teams, but how much time and effort is required to generate results for this analysis? Not even mentioned the involved human error.

Now another perspective: suppose that one or more connections show many problems as shown in Figure 15 (digital signal ringing). You now need to modify the network

and re-evaluate the new design! With an automated system, all the measurements are done in a few hours or even some minutes. Automatization gives not only the possibility of making measurements with a resulting verdict but also pictures can be generated for each measurement within the final report, which gives a verdict for each measurement. Example pictures with 5 dominant bits followed by a recessive bit (2Mbit/s) are Figure 14 and Figure 15.

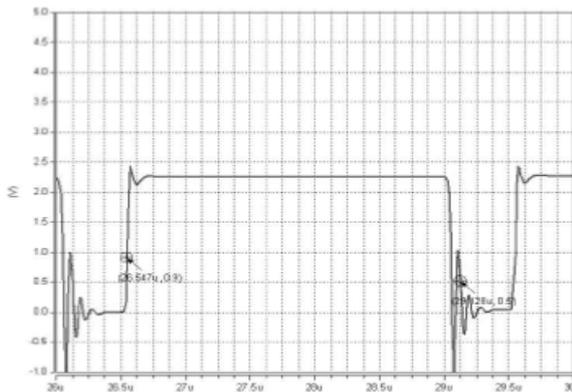


Figure 14: Automated analog measurement

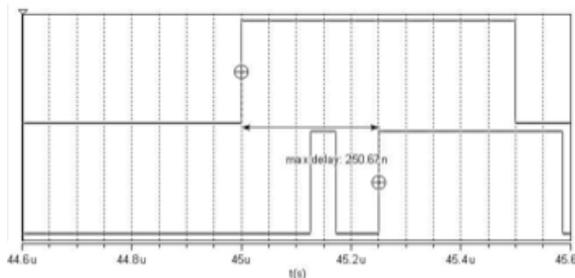


Figure 15: Automated digital measurement

## Conclusion

Recent technology applied to the classic CAN bus allows to perform a communication with a higher data rate and even larger payloads. Simulation nowadays is an excellent approach to overcome the design problems at an early stage of a vehicle development and/or newer versions of existent designs. The higher data transmission rate makes the asymmetry on different signals within a network a key to success and its evaluation is achievable by means of simulation.

On the other side, while simulation alone plays an important role for new CAN-FD challenges, automatization is what makes a difference regarding the effectiveness and efficiency of a project. With automatization, not only huge

networks can be evaluated but also marginal behaviors due to production tolerance and temperature coefficients are contemplated, thus overcoming problems in components and transceivers, preventing the designer of falling in such situations.

With an automatized simulation environment, a topology can be evaluated to different real possible conditions, where different parts of the topology can be exposed to different temperatures, components of each node are affected to fabrication tolerances, cables are affected to different temperatures, clock deviation is maximal in some nodes and minimal in others and so on.

Simulation through automatization makes it possible for the CAN-FD IVN topology designer to manage such effort in a topology validation, resulting in a real a possibility that was not so easily accessible before. The cost reduction and the broad analysis are 2 key points that will make your designs better than ever before.

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