Part I – CAN XL physical layer network design

With CAN XL protocol in combination with the CAN SIC XL transceiver bit rates up to 20 Mbit/s are possible. In two articles, the author presents testing results of this transmitter concept in different network topologies.

The new transmitter concept in the data phase was necessary to achieve bit rates above 8 Mbit/s. In a special physical layer plugfest in January 2023 in Nuremberg (Germany), this concept was tested in different network topologies.

Topology investigations

During the plugfest, the following topologies were verified, in order to evaluate the maximum possible bit rate:

- Point-to-point network with different distances between the nodes;
- Daisy-chain topology as used in 10BaseT1S networks with different distances between nodes;
- Linear topology with different stub lengths;
- Single-star topology;
- Multi-star topology.

In this article the testing results of the topologies as illustrated in Figure 1 to Figure 3 are presented:

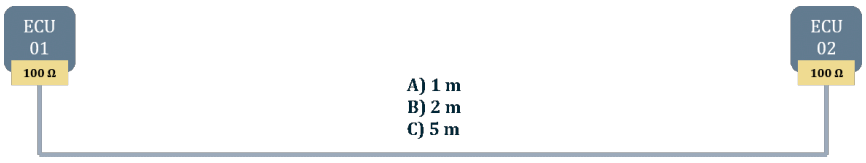

Figure 1: Point-to-point network (Source: Infineon)

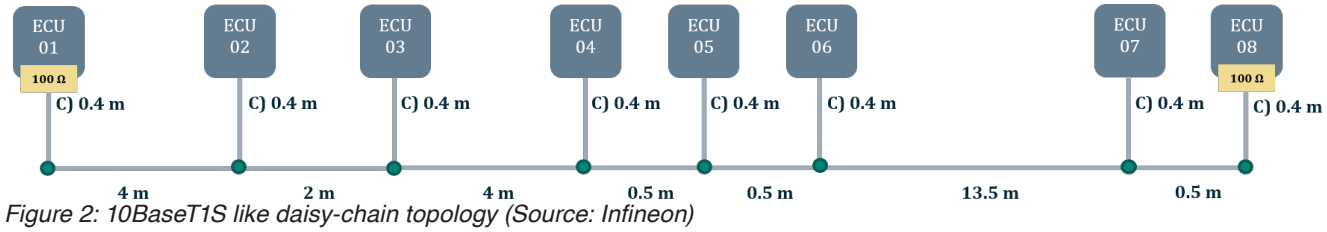

Figure 2: 10BaseT1S like daisy-chain topology (Source: Infineon)

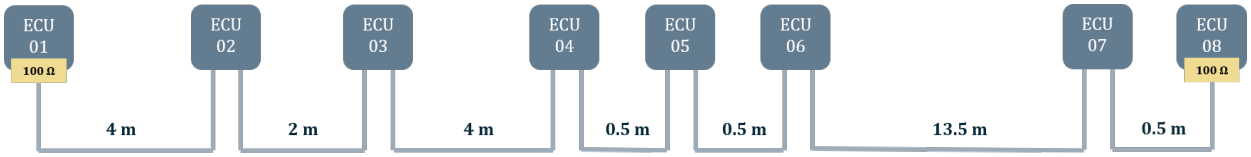

Figure 3: CAN typical linear topology with short stub lengths (Source: Infineon)

In the second article (to be published in CAN Newsletter 2-2025) the testing results of the topologies as illustrated in Figure 4 to Figure 6 will be presented.

The verified pattern

The most critical scenarios in the CAN XL frame transmission are:

- The transition from SIC (signal improvement capability) mode to FAST mode;
- A burst of short bits;
- A short bit after a long level_0 phase or a long level_1 phase (maximum 11 bit due to the stuff bit rule) with the opposite level.

During the ADH (arbitration to data high) bit, the transmitter switches from dominant state to level_0 and afterwards to level_1 (see Figure 7). In parallel, all receiving nodes change the receiver thresholds. This is caused by PWM-coded (pulse-width modulation) symbols sent from the CAN XL protocol controller to the TXD pin of the transceivers. Before the PWM-coded symbol on the TXD pin is detected the receiving nodes transmit a short dominant pulse followed by a shortened SIC phase. The requirement is, that level_1 is stable before the SDT (service data unit type) field starts. Also, the length ▷

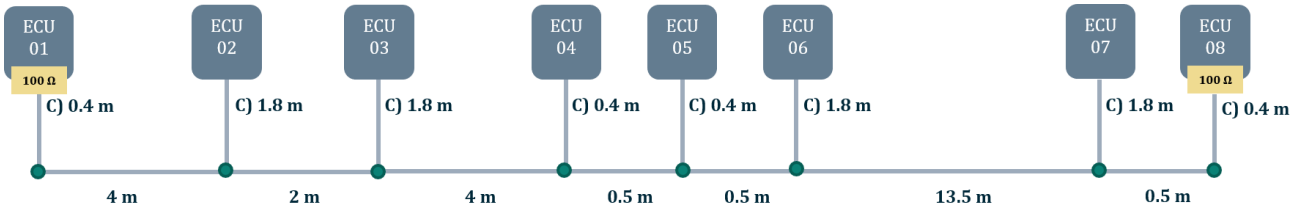

Figure 4: CAN typical linear topology with different stub lengths (Source: Infineon)

of the DL1 (data low) bit is of interest. The transition from DH2 (data high) to DL1 is used for resynchronization of the CAN XL protocol controller after the transition into the data phase. Also, level_0 should be achieved. In the SDT field a "0101" bit pattern was chosen to analyze the impact of short bits in case of high bit rates.

A long phase (four consecutive bits) followed by short bits (one, two, or three) with the opposite level (see Figure 8): The objective was to find out, how long it takes, until the bus signals are stable, especially at high bit rates. The bit lengths are measured after a longer level_0 or level_1 phase and the impact of the length on the following bits.

One bit after 11 consecutive level_1 or level_0 bits (highest possible number of consecutive bits) (see Figure 9): The objective was to find out, how the bit length and the level behave after the longest possible phase in the frame.

The test topology 1c (see Figure 11) is a point-to-point network. The distance between the two nodes is 5 m. The bit rate is 20 Mbit/s. There were observed no reflection or jitter during the full FAST phase (see Figure 12), which was short in this test. The values of level_0 and level_1 are independent of the bit length.

Figure 13 shows the critical ADS (arbitration to data sequence) phase, consisting of ADH bit (2000 ns), DH1 (data high; 50 ns), and DH2 bit (50 ns). At the beginning of the transition from dominant to level_0 a short SIC phase of the transmitting node can be seen, before the transceiver has the new PWM coding detected. The length and the voltage swing of this spike depends on the duty-cycle ratio of the PWM symbol. After the transition to level_1, the short spike is coming from the receiving node. On the receiving node, the PWM coding causes to set the transceiver into

The test criteria

The bit-time lengths (see Figure 10) were measured at +100-mV and -100-mV thresholds. The bit time should be lose to the nominal bit time or multiples of them. For high bit rates the 0-V threshold was used. Glitches with a length of 20 ns were ignored.

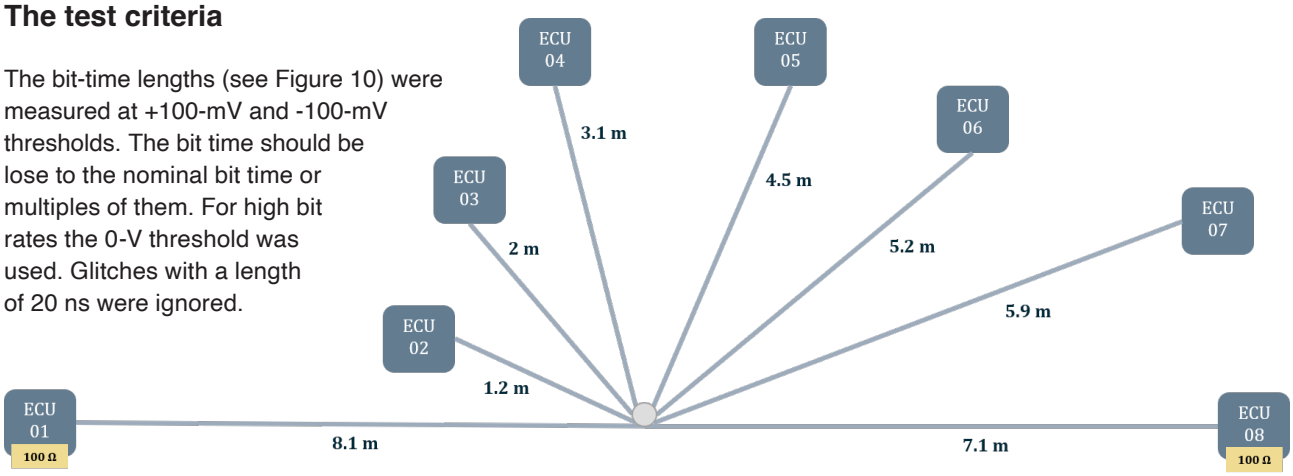

Figure 5: Single-star topology with stub lengths of 1 m, 2 m, and 4 m (Source: Infineon)

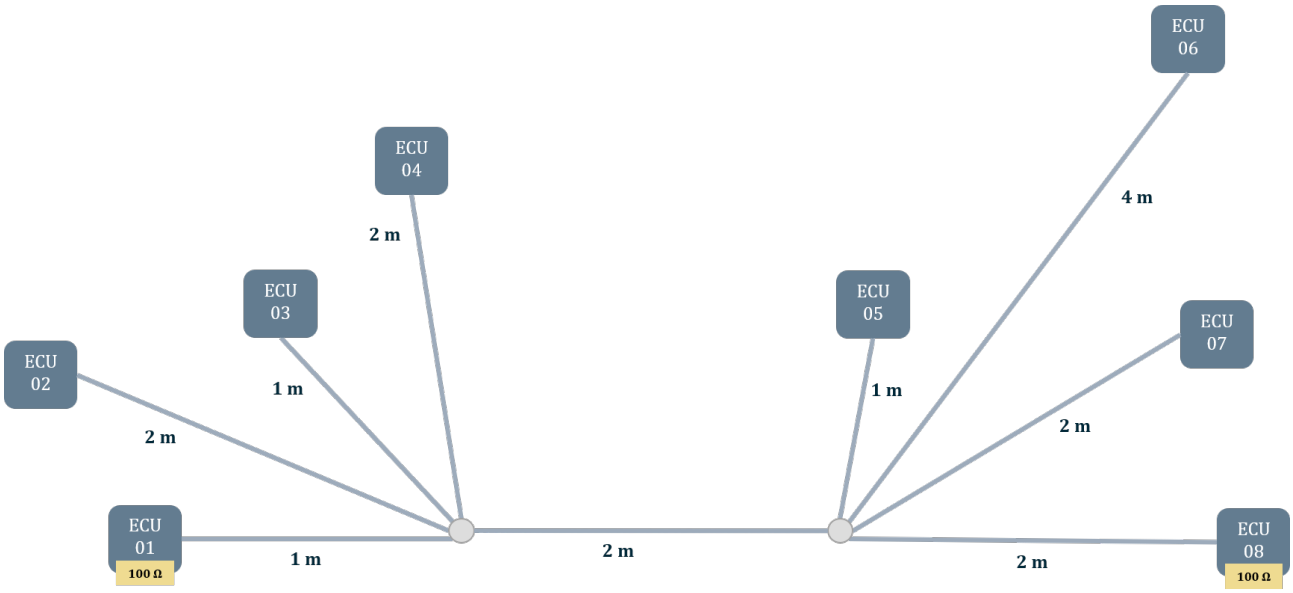

Figure 6: Multi-star topology (Source: Infineon)

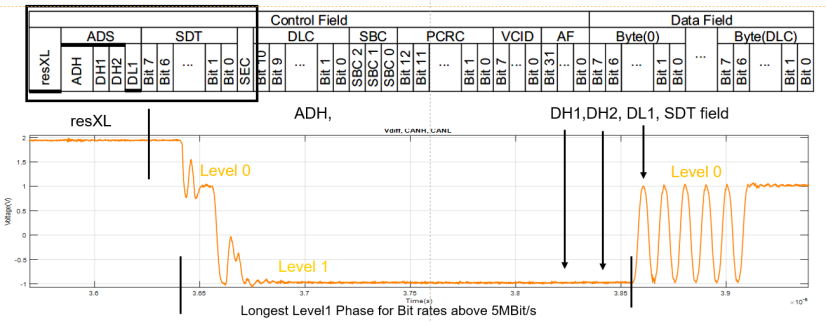

Figure 7: SIC-mode to FAST-mode transition during ADS field (Source: Infineon)

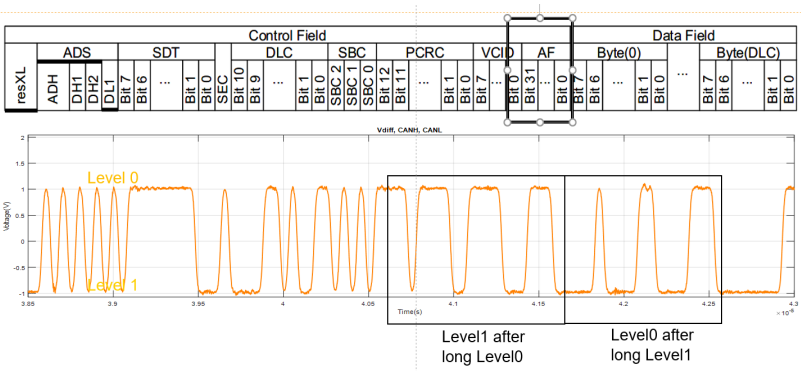

Figure 8: One, two, or three bits with opposite level after a long level_0 or a long level_1 sequence (Source: Infineon)

FAST mode. Before the transceiver is able to detect PWM coding on its TXD pin, a short dominant pulse followed by a shortened SIC phase is transmitted. The spikes during the transition from level_0 to level_1 are very short. The level_1, level_0 pattern in the SDT field are without any observations, too.

The maximum voltage values on single bits of level_0 or level_1 are achieved but they are short. In the transceiver prototype samples were used. The slew rates of non-prototype transceivers might be faster and the maximum-level phase during a single bit might be longer.

Using test topology 3 (see Figure 15), symbol levels in FAST mode and pulse (bit) lengths are symmetric. In scenario 1, node 7 transmitted with 20 Mbit/s (see Figure 16). Voltage level of short bits did not achieve the maximum voltage values of level_0 and level_1. There were just low (but acceptable) bit-time degradations observed. Temperature dependencies and wire-impedance variations were not considered and should be verified separately.

In scenario 2 of test topology 3 (see Figure 17), node 3 transmits frames and node 7 receives them. The maximum bit rate, which has been used successfully is 20 Mbit/s. In this test setup, the impact of the distance between transmitter and receiver is analyzed. The parasitic capacitance on the ECUs (electronic control unit), the number of star points, the high number of untwisted parts, and the 28-m distance between the transmitter and receiver were of interest. Node 3 transmits the pulse (bit) at first into the wire impedance of 100 Ω, with a delay the impact of the termination on node 1 (delay round about 40 ns (7 m x 5,5ns/m)) can be observed and with a delay of 120 ns (20 m x 5,5 ns/m) can be seen. The single-bit bursts are the most interesting situations during the frame transmission.

As seen in Figure 18, the longer distance between transmitting and receiving node caused lower voltage levels of short bits and didn't achieve the maximum voltage values of level_0 and level_1. The bit length is shorter but close to the minimum bit length. In the single-bit burst a "king of pumpkins" can be seen. The first bit level is lower than the second one and the third one, caused by the capacitive load. The capacitance on the ECUs should be as low as possible. The critical situation is the single bit after multiple bits with the same level. The level has an acceptable distance to 100 mV (maximum voltage value of the receiver threshold). There are impacts of temperature dependencies as well as wire-impedance variations due to production and mechanical stress. Also, the overall length of the untwisted parts has an impact on the maximum voltage values and the bit-length symmetry. These impacts are minor: The bit-time degradation is acceptable.

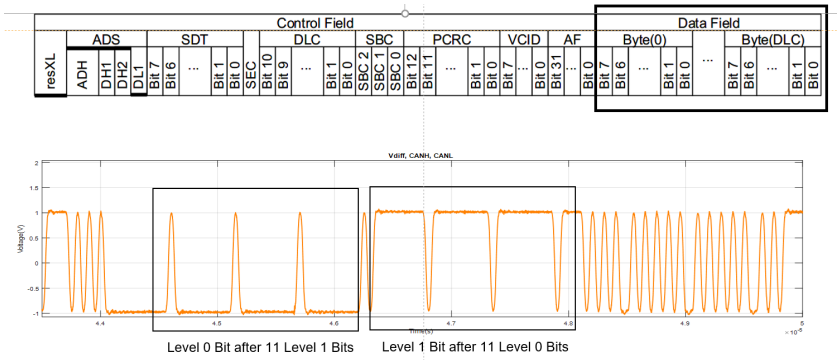

Figure 9: Level_1 or level_0 bit after a long phase (Source: Infineon)

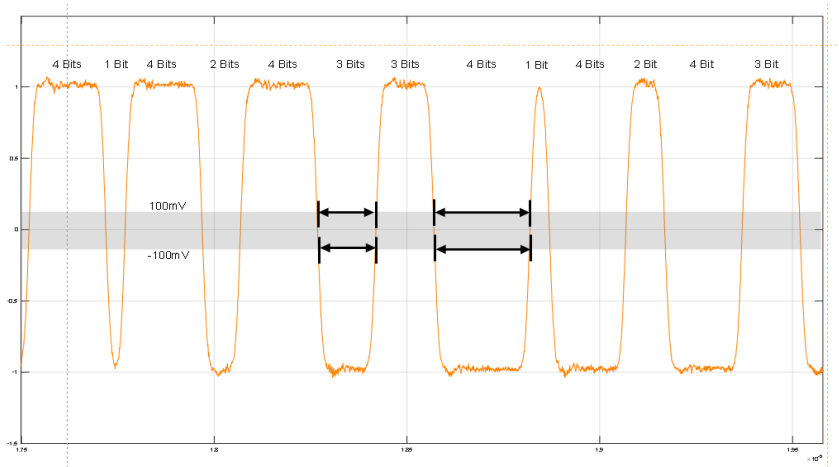

Figure 10: Test criteria timing (Source: Infineon)

In the scenario shown in Figure 19, the impact of terminated node was of interest. The impedance scenario of the transmitting node is different to the unterminated node. The transmitter is directly connected to the 100-Ohm termination resistor and in parallel with the 100-Ohm impedance of the wire. The impact of the second termination located in node 1 can be observed after 150 ns during the third bit. The waveforms on node 7 are more or less the same as on node 8 due to the short distance between both nodes. The voltage level of short bits doesn't achieve the maximum voltage values of level_0 and level_1. The low bit-time degradation is acceptable.

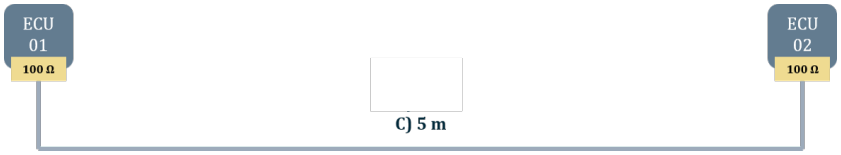

Figure 11: Test topology 1c (Source: Infineon)

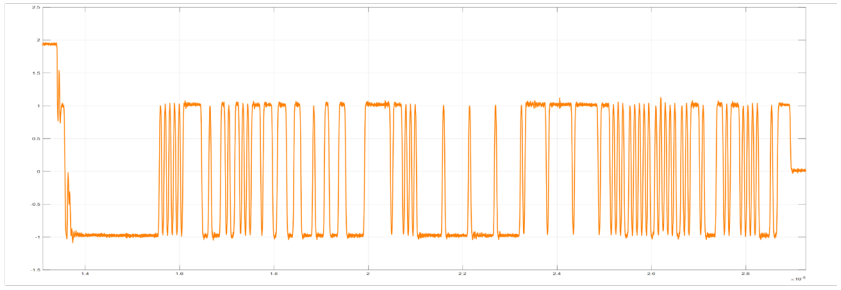

Figure 12: Full FAST phase result (differential network signal) for test topology 1c (Source: Infineon)

The long wire length, the number of nodes, the parasitic capacitances, and the untwisted parts caused that the voltage levels of short bits don't achieve the maximum values of level_0 and level_1. The bit lengths were shortened but close to the nominal bit time. In the test, the used prototype transceivers didn't fulfill all requirements, especially the slew-rate condition. With final silicon, the results might be better, the low bit-time degradation is acceptable.

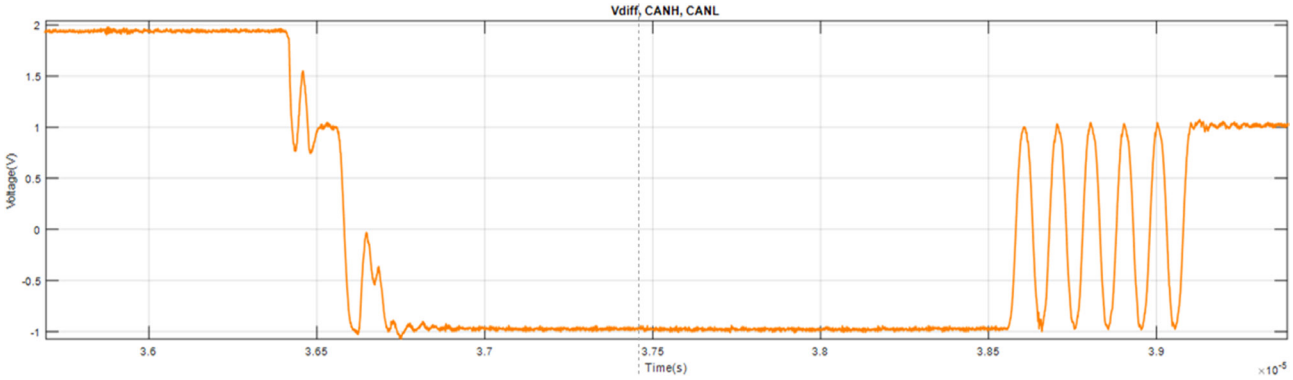

Figure 13: ADS phase and SDT phase results (Source: Infineon)

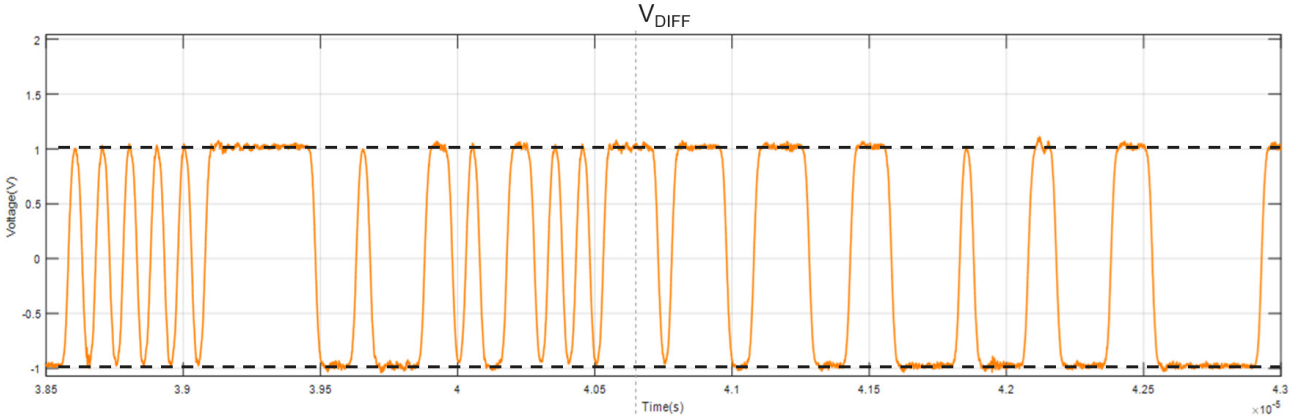

Figure 14: Different pattern in FAST mode (Source: Infineon)

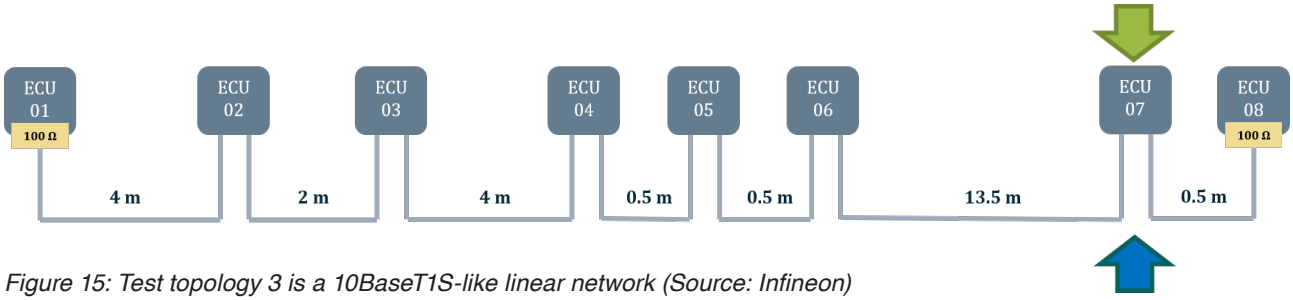

Figure 15: Test topology 3 is a 10BaseT1S-like linear network (Source: Infineon)

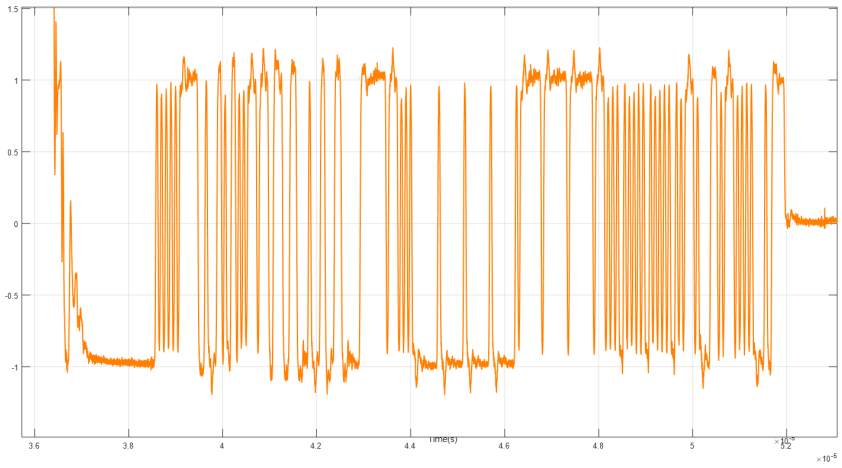

Figure 16: Full FAST phase on node 7 (Source: Infineon)

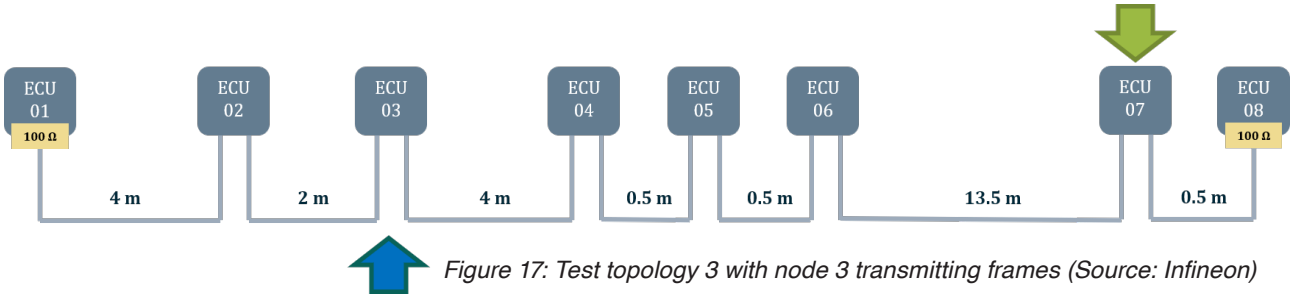

Figure 17: Test topology 3 with node 3 transmitting frames (Source: Infineon)

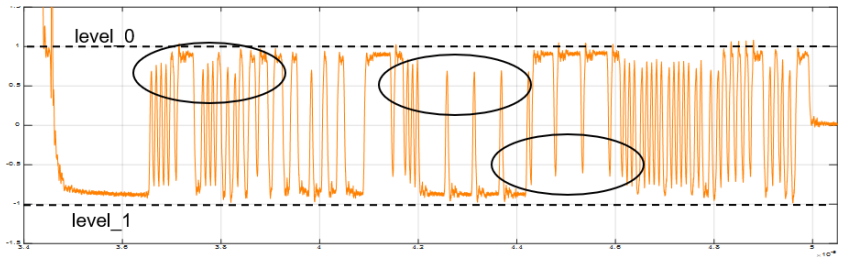

Figure 18: Full FAST phase of node 3 when transmitting (Source: Infineon)

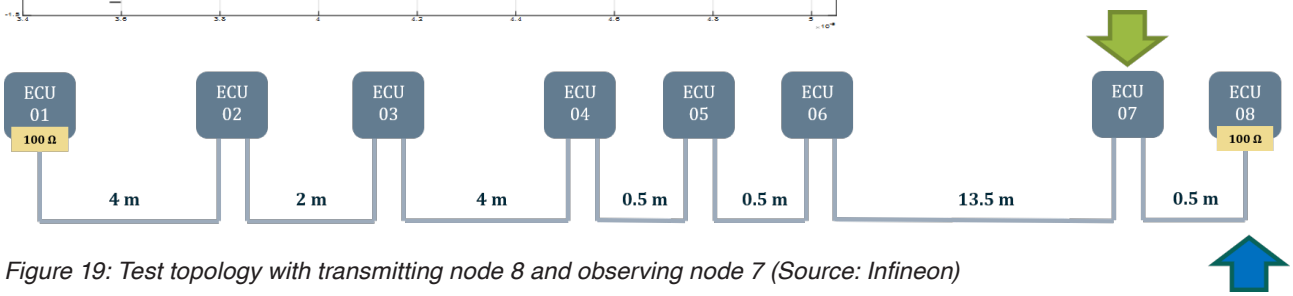

Figure 19: Test topology with transmitting node 8 and observing node 7 (Source: Infineon)

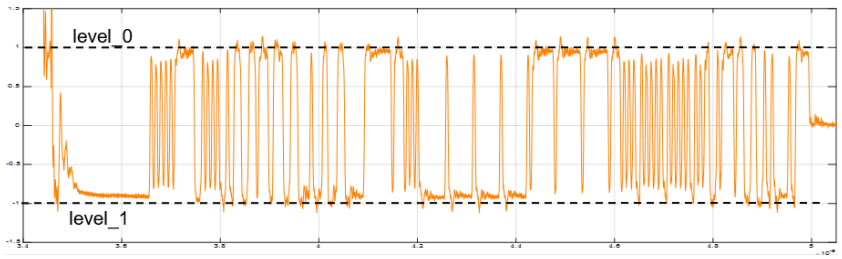

Figure 20: Full FAST phase of the transmitting node 8 (Source: Infineon)

Conclusion

In this first article, three tested CAN XL network topologies and according results have been presented. These topologies were the point-to-point network, the 10BaseT1S-like daisy-chain topology, and a CAN-typical linear topology with short stub lengths. In the second article (to be published in CAN Newsletter 2-2025) the testing results of three further topologies will be presented. These are the CAN-typical linear topology with different stub lengths, a single-star topology with different stub lengths, and a multi-star topology. ◀

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